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Appl. No. 10/073,550

Amendment Dated April 7, 2004

Reply to Office Action of January 7, 2004

In the Claims:

Claim 1 (Currently Amended). In a dual damascene patterning process, an etching method which comprises:

providing a semiconductor structure with functional elements formed in a substrate, a dielectric disposed on the substrate, a photoresist etching mask above the dielectric, and a polymer intermediate layer between the etching mask and the dielectric layer;

etching the dielectric layer and the polymer intermediate

layer for the dual damascene patterning with a CF4 ARC open

process with high selectivity with respect to the photoresist

of the etching mask, said CF4 ARC open process including:

adjusting RF power between 550 and 650 watts, adjusting pressure between 80 and 120 mtorr, adjusting CF₄ flow between 35 and 45 sccm, adjusting CHF₃ flow between 17 and 23 sccm, adjusting Ar flow between 80 and 120 sccm, and adjusting O₂ flow between 5 and 7 sccm.

Claim 2 (Original). The etching process according to claim 1, wherein the dielectric is an oxide layer.

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Claim 3 (Original). The etching process according to claim 1, which comprises setting an etching time to at least twice an etching time of an O2/N2 ARC open process.

Claim 4 (Original). The etching process according to claim 3, which comprises setting the etching time, depending on an etching depth, to approximately 140 s.

Claim 5 (Original). The etching process according to claim 1, which comprises performing the etching process in an etching chamber with plasma assistance.

Claim 6 (Original). The etching process according to claim 5, which comprises etching with an RF power of approximately 600 watts.

Claim 7 (Canceled).

Claim 8 (Original). The etching process according to claim 7. which comprises setting a CF4 flow during the ARC open process to approximately 40 sccm and setting the CHF3 flow to approximately 20 sccm.

Claim 9 (Currently Amended). An etching process for oxide patterning in a semiconductor structure, which comprises:

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providing a substrate with functional elements formed therein, an oxide layer on the substrate, an etching mask formed of a photoresist above the oxide layer, and a polymer intermediate layer forming an antireflection layer between the etching mask and the oxide layer;

patterning the oxide layer during a dual damascene patterning for a metallization;

etching the polymer intermediate layer and the oxide layer in a common CF4/CHF3 etching process with high selectivity with respect to the photoresist; and , the etching process including:

thereby adjusting an etching-gas flow for CF_4 to 35 - 45 secm and an etching gas flow for CHF_3 to 17 - 23 secm in the common etching process.

adjusting RF power between 550 and 650 watts, adjusting pressure between 80 and 120 mtorr, adjusting CF₄ flow between 35 and 45 sccm, adjusting CHF₃ flow between 17 and 23 sccm, adjusting Ar flow between 80 and 120 sccm, and adjusting O₂ flow between 5 and 7 sccm.

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Claim 10 (Original). The etching process according to claim 9, which comprises setting the etching time, depending on an etching depth, to approximately 140 s.

Claim 11 (Original). The etching process according to claim 9, which comprises performing the etching process in an etching chamber with plasma assistance.

Claim 12 (Original). The etching process according to claim 11, which comprises etching with an RF power of approximately 600 watts.

Claim 13 (Original). The etching process according to claim 9, which comprises setting the etching gas flow for CF_4 to approximately 40 sccm and the etching gas flow for CHF_3 to approximately 20 sccm in the common etching process.

Claim 14 (Canceled).